Remarks

Although no formal objection or rejection was stated, 35 USC 112(2) has been referenced by the Examiner to preface a discussion in which the term "observable", and its grammatical variations, are deemed to be vague and ambiguous in the context of a processor. The Examiner uses the terms "observe" and "see" as synonyms, and Applicants agree with this. However, Applicants disagree that the specification does not sufficiently redefine the terms.

In the text from page 4 line 22 to page 5 line 15 of Applicants' specification, the term "see", and by association its synonym "observe", is defined within the context of memory operation ordering by multiple processors. In this definition, a store (write) operation to a memory location by a first processor is 'seen' (observed) by a second processor if a load (read) of that same location by the second processor reads the value stored by the first processor. Similarly, a load operation by the first processor is seen by the second processor if a write operation by the second processor does not affect the value read by the first processor, i.e., if the value read by the first processor is the value that was in that location before the write by the second processor.

Claims 1-41 have been rejected under 35 USC 102(a) as being anticipated by pages 15-26 of the publication "Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors" ("Gharachorloo").

Claims 42-45 have been rejected under 35 USC 103(a) as being unpatentable over Gharachorloo.

Applicants respectfully traverse these rejections because the cited references do not disclose or suggest every element of any pending claim, as the following analysis shows.

Independent claims 1, 23, and 42 each recites dividing a memory system into multiple regions, and applying the remaining limitations only to that region. The limitation of multiple regions was previously found in claims 4 and 34, which have now been cancelled as redundant, and may also be found in the specification at page 4 lines 9-11, page 7 lines 8-12, page 7 line 21 – page 8 line 2, and page 8 lines 8-12. The limitation of multiple regions, although it appeared in some of the original claims, was never addressed in the rejection. Gharachorloo does not disclose or suggest dividing the memory system into multiple regions and applying the ordering operations specifically to a particular region.

The remaining dependent claims each depend directly or indirectly from one of claims 1, 23, or 42, and therefore contain the same limitations that are not found in the cited reference. The remaining dependent claims were amended only to assure compatibility with the multiple region limitation that is now in the independent claims, and to correct minor, previously undetected, inconsistencies with antecedent basis.

Reconsideration and withdrawal of the rejection of the claims is respectfully requested.

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Conclusion

For the foregoing reasons, it is submitted that the application is in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. If any fee insufficiency or overpayment is found, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

Intel Corporation

Date: January 23, 2007

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